the output condition and accumulated period data of the pulse counting circuit 173 are reset after the predetermined time has passed. Thereby, malfunction of power generation control can be prevented.

The high voltage pulse generated in this case is absorbed by the power Zener diode forming the full-wave rectifier 4. As explained above, the reverse withstand voltage of power Zener diode is thermally designed particularly to be resistive to the condition for instantaneously generating a non-load saturation voltage of the alternator 1 with cut-off of the rated load under the maximum allowable number of rotations of the alternator 1 and therefore such high voltage pulse can be absorbed with sufficient allowance.

In addition, since the timer circuit 183 for resetting the data of the accumulated period can set the time independently, the connection failure of the power supply line 8 and chattering phenomenon when the load is cut off can be discriminated easily.

[Fourth Embodiment]

Fig. 17 shows a high voltage pulse detecting circuit 83 of the alternator 1 according to a fourth embodiment. This circuit 83 is structured with a high voltage pulse detecting section 160, discriminating section 170 and output control section 180.

The discriminating section 170 is similar to that of the third embodiment, but it further comprises an OR gate 184, an inverter 185 and an AND gate 186. The discriminating section 170 generates a reset pulse signal with the timer circuit 171

to input this signal to the one input terminal of the AND gate 186 and also inputs the signal inverted with the inverter 185 from the output signal of the pulse duration measuring circuit 175 to the other input terminal of the AND gate 186. The output signal of the AND gate 186 is inputted to the OR gate 184.

Fig. 18 shows signal waveforms to be inputted to each section of the high voltage pulse detecting circuit 83 shown in Fig. 17, wherein the high voltage pulses are generated several times.

When a high voltage pulse higher than the reference voltage V3 is generated several times, the output of the voltage comparator 66 becomes high level corresponding thereto. With the rising edge of this output signal, the timer circuit 171 is triggered to operate. The AND gate 172 passes, during operation of the timer circuit 171, the output signal of the voltage comparator 66 to the pulse counting circuit 173 of the next stage. Here, the pulse counting circuit 173 outputs the signal of high level for the input of the second and subsequent pulses. Therefore, the output of the AND gate 174 becomes high level only for the pulse duration. The pulse duration is measured and accumulated with the pulse duration measuring circuit 175. When generation of high voltage pulse stops, operation of the timer circuit 171 also stops and the reset pulse of the timer circuit 171 is generated (Fig. 18(k)).

The output of the pulse duration measuring circuit 175 maintains the low level because the accumulated period of pulse does not reach the predetermined value (for example, 50ms). The

signal of the high level that is generated by inverting such a signal with the inverter 185 is then inputted to the AND gate 186. In this case, as the output of the AND gate 186, the reset pulse of the timer circuit 171 is outputted directly. Since the timer circuit 181 is not operative, the reset pulse outputted from the timer circuit 181 maintains the low level. Therefore, the OR gate 184 passes directly output of the AND gate 186 to the circuit of the next stage. Thereby, the reset pulse outputted from the timer circuit 171 is sent to the pulse duration measuring circuit 175 and the pulse counting circuit 173 to reset the accumulated period data and pulse count number.

Fig. 19 shows signal waveforms inputted to each section of the high voltage pulse detecting circuit 83 shown in Fig. 17. In this case, the high voltage pulses are generated continuously.

When high voltage pulses are applied, the pulse durations are measured and accumulated with the pulse duration measuring circuit 175 (Fig. 19(g)). When the high voltage pulses are applied continuously, since the timer circuit 171 does not operate during this period, the reset pulse is not generated with the timer circuit 171. Thereafter, when the pulse duration exceeds the predetermined accumulated period (for example, 50 msec), the output of the pulse duration measuring circuit 175 becomes high level and thereby the timer circuit 181 operates. The output control circuit 182 controls power generation while the timer circuit 181 operates (for example, 1 sec).

Upon completion of the timer circuit 181, the timer reset pulse 181 outputs the reset pulse (Fig. 19(n)). When power